

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1 to 6. (Canceled)

1 7. (Currently Amended) A data transfer system comprising:
2 a plurality of first bus devices, at least one first bus
3 device being a first bus data supplying device capable of supplying
4 data, at least one first bus device being a first bus data
5 receiving device capable of receiving data, at least one first bus
6 device being a first bus master device capable of requesting and
7 controlling data transfer and at least one first bus
8 supplying/receiving device being a central processing unit which is
9 further capable of controlling data transfer;
10 a first data bus connected to each of said plurality of first
11 bus devices and capable of transferring data from a first bus data
12 supplying device to a first bus data receiving device under control
13 of a first bus master device;
14 a plurality of second bus devices, at least one second bus
15 device being a second bus data supplying device capable of
16 supplying data, at least one second bus device being a second bus
17 data receiving device capable of receiving data, a plurality of
18 second bus devices each being a second bus master device capable of
19 requesting and controlling data transfer, a predetermined one of
20 said plurality of second bus devices being a dominant second bus
21 master device responsive to real time events asynchronous to
22 operation of said central processing unit;
23 a second data bus connected to each of said plurality of
24 second bus devices and capable of transferring data from a second
25 bus data supplying device to a second bus data receiving device
26 under control of a second bus master device;

27 a bus bridge connected to said first data bus and said second
28 data bus, said bus bridge capable of supplying data to said first
29 bus, receiving data from said first bus, supplying data to said
30 second bus, receiving data from said second bus, not capable of
31 controlling data transfer on said first bus and capable of
32 controlling data transfer on said second bus; and

33 a second bus arbiter connected to each of said at least one
34 second bus master device, said second bus and said bus bridge, said
35 second bus arbiter granting control of data transfer on said ~~first~~
36 second bus to one and only one of the set of devices including each
37 second bus master and said bus bridge, said second bus arbiter
38 granting control of data transfer to said dominant second bus
39 master immediately upon request and interrupting any data transfer
40 controlled by another second bus master.

1 8. (Previously Presented) The data transfer system of claim
2 7, wherein:

3 said at least one first bus master device consists of a direct
4 memory access unit.

1 9. (Previously Presented) The data transfer system of claim
2 7, wherein:

3 at least one first bus supplying/receiving device consists of
4 a memory which is not capable of controlling data transfer.

1 10. (Previously Presented) The data transfer system of claim
2 7, wherein:

3 each second bus master generates a corresponding bus request
4 signal to said second bus arbiter for second bus to request control
5 of said second bus, said second bus arbiter having grant logic
6 corresponding to each second bus master supplying a bus grant
7 signal to said corresponding bus master upon bus grant, said bus

8 request signal of said dominant bus master supplied to said grant
9 logic corresponding to every other second bus masters for
10 inhibiting generation of said grant request.

1 11. (Previously Presented) The data transfer system of claim
2 10, wherein:
3 said bus arbiter grants control of said second bus to second
4 bus master devices other than dominant bus master in a round robin
5 fashion.